REMARKS

Claims 1-15 are pending. Claims 1, 2, and 13 have been amended. In particular, claim 1 has been amended to recite the step of modifying the allocation and circuit information. Support for this amendment can be found *e.g.* on page 9, lines 36-37, page 10, lines 1-5, and in Figures 1, 5A, and 5B. Claim 2 has been amended to track claim 1. Editorial revisions have been made to claim 13. No new matter has been added. Applicants respectfully request reexamination and allowance of claims 1-15.

CLAIM REJECTIONS

Claims 1-15 have been rejected under 35 U.S.C. 102(e) as being anticipated by Okada *et al.* (US 6,604,232, hereinafter "Okada"). Claims 2-15 depend from claim 1. Applicants respectfully assert that claim 1 is patentable over Okada.

Claim 1 recites, in part, a high-level synthesis method including generating initial allocation information and initial circuit information and modifying the allocation and circuit information. The allocation information and circuit information are modified based on resource-level layout information representing a layout of the resources. Examples of resource-level layout information are shown *e.g.* in Figures 7-9, 18-20, 23, and 26 of the present application.

Okada discloses a high-level synthesis method including generating a CDFG, modifying the CDFG based on logical synthesis, scheduling the CDFG, and then allocating logic circuits to execute the CDFG. *See e.g.* column 8, lines 1-10 and Figure 12. Okada fails to disclose or suggest modifying the allocation information after it has been initially generated. Rather, Okada is directed to the modification of the CDFG through logical synthesis before the steps of scheduling or allocation. *See id.* Okada further fails to disclose or suggest generating allocation information based on resource-level layout information. Rather, allocation information is generated based on the operating time of the logically synthesized and scheduled CDFG information. *See e.g.* column 4, lines 41-51. In addition, applicants respectfully point out that Figures 27-43 do not depict resource level layout information. Rather, Figures 27, 30-33, 35, 38, 39, 41, and 42 in Okada depict CDFGs and scheduled CDFGs and Figure 29 depicts a flow chart. Figures 28, 34A, 34B, 36, 40, and 43 depict circuit diagrams and Figure 37 depicts an operational description of a circuit. Therefore, Okada does not anticipate claim 1. Claims 2-15

are allowable for at least the same reasons. Applicants respectfully request allowance of claims 1-15.

In view of the above amendments and remarks, Applicant respectfully requests a Notice of Allowance. If the Examiner believes a telephone conference would advance the prosecution of this application, the Examiner is invited to telephone the undersigned at the below-listed telephone number.

Respectfully submitted,

MERCHANT & GOULD P.C.
P.O. Box 2903
Minneapolis, Minnesota 55402-0903
(612) 332-5300

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Douglas P. Mueller
Reg. No. 30,300

DPM/JKS/jt